Application No.: 09/387,857 Docket No.: 21776-00039-US

AMENDMENTS TO THE CLAIMS

This listing of the claims will replace all prior versions, and listings, of claims in the application:

Claims 1-27 cancelled.

28. (Allowed) A method of fabricating a semiconductor device, comprising:

the first step of defining an element active region by forming an element isolation structure on a semiconductor substrate;

the second step of forming an insulating film on said semiconductor substrate in said element active region;

the third step of forming a first conductive film on an entire surface of said semiconductor substrate including said insulating film, and said element isolation structure;

the fourth step of forming a mask pattern having first and second openings on said first conductive film;

the fifth step etching said first conductive film until said element isolation structure is exposed in said first opening by using said mask pattern as a mask, thereby dividing said first conductive film, and simultaneously forming a recess in said second opening where said first conductive film forms a bottom of said recess;

the sixth step of forming a dielectric film so as to cover a surface of said firs conductive film; and

the seventh step of forming a second conductive film on said dielectric film opposing said first conductive film through said dielectric film.

29. (Allowed) A method according to claim 28, further comprising, after the seventh step, the eighth step of doping an impurity into said semiconductor substrate in said element active region to form a pair of impurity diffusion layers in surface regions of said semiconductor substrate on two sides of said first conductive film.

30. (Allowed) A method according to claim 28, wherein in the fourth step, said mask pattern is so formed that a width of said first opening is not less than twice a width of said second opening.

31. (Allowed) A method according to claim 28, further comprising, between the third and fourth steps, the ninth step of planarizing said first conductive film by polishing, and

wherein in the fourth step, said mask pattern is so formed that said second opening is positioned above said element active region.

Claims 32-35 cancelled

36. (Currently amended) A method of fabricating a semiconductor device, comprising:

the first step of forming a first conductive film in an insulating film region on a semiconductor substrate;

the second step of forming a mask pattern having [two] first and second openings of different dimensions on said first conductive film;

the third step of etching said first conductive film by using said mask pattern as a mask, thereby dividing said first conductive film conforming to a shape [of one] of said first [openings] opening so as to reach said insulating film region, and simultaneously forming a cylindrical hole below said second opening in which a surface of said

insulating film region is exposed[, and simultaneously forming at least one recess] in a surface of said divided first conductive film conforming to a shape of the other opening;

the fourth step of forming an insulating film so as to cover a surface of said first conductive film; and

the fifth step of forming a second conductive film so as to cover a surface of said insulating film opposing said first conductive film through said insulating film.

37. (Original) A method according to claim 36, wherein in the third step, said recess is so formed as to reach said insulating film region, thereby forming a hole in which a surface of said insulating film region is exposed.

38. (Allowed) A method of fabricating a semiconductor device, comprising:

the first step of defining an element active region by forming an element isolation structure on a semiconductor substrate;

the second step of forming an insulating film on said semiconductor substrate in said element active region;

the third step of forming a first conductive film on an entire surface including said insulating film and said element isolation structure;

the fourth step of forming a mask pattern having at least first and second openings on said first conductive film;

the fifth step of etching said first conductive film until said element isolation structure is exposed in said first and second openings by using said mask pattern as a mask, thereby dividing said first conductive film below said first opening, and simultaneously forming a cylindrical hole extending through said first conductive film below said second opening and said first conductive film is etched until said insulating layer is exposed in said first opening;

the sixth step of forming a dielectric film so as to cover said first conductive film; and

the seventh step of forming a second conductive film on said dielectric film and opposing said first conductive film through said dielectric film.

39. (Allowed) A method according to claim 38, further comprising, after the seventh step, the eight step of doping an impurity into said semiconductor substrate in said element active region to form a pair of impurity diffusion layers in surface regions of said semiconductor substrate on two sides of said first conductive film.

40. (Allowed) A method according to claim 38, further comprising, between the third and fourth steps, the ninth step of planarizing said first conductive film by polishing.

41. (Allowed) A method according to claim 38, wherein in the first step, a field shield element isolation structure in which a shield plate electrode is embedded is formed on said semiconductor substrate.

42. (Allowed) A method of fabricating a semiconductor substrate, comprising:

the first step of defining an element active region by forming an element isolation structure on a semiconductor substrate;

the second step of forming a gate oxide film and a gate electrode on said semiconductor substrate in said element active region;

the third step of doping an impurity into said semiconductor substrate in said element active region to form a pair of impurity diffusion layers in surface regions of said semiconductor substrate on two sides of said gate electrode;

the fourth step of forming an insulating interlayer on an entire surface of said semiconductor substrate;

the fifth step of forming a hole in said insulating interlayer in which one of said impurity diffusion layers is exposed;

the sixth step of forming a first conductive film on said insulating interlayer which fills said hole electrically connected to one of said impurity diffusion layers;

the seventh step of forming a mask pattern having at least first and second openings on said first conductive film;

the eighth step of etching said first conductive film by using said mask pattern as a mask, thereby dividing said first conductive film below said first opening, and simultaneously forming a cylindrical hole extending through said first conductive film below said second opening, said first conductive film is etched until said insulating interlayer is exposed in said first opening;

the ninth step of forming a dielectric film so as to cover a surface of said first conductive film; and

the tenth step of forming a second conductive film so as to cover said dielectric film opposing said first conductive film through said dielectric film.

43. Cancelled

44. (Allowed) A method according to claim 42, further comprising, between the sixth and seventh steps of planarizing said first conductive film by polishing.

45. (Allowed) A method according to claim 42, wherein in the first step, a field shield element isolation structure in which a shield plate electrode is embedded is formed on said semiconductor substrate.

Claims 46-47 cancelled